CLAIMS

1. A process for management of a Test Access Port function in a plurality of components arranged on a single chip, each of said components provided with a respective TAP function adapted to be driven by a respective clock and by at least one further signal, comprising the operations of:

using said at least one further signal in a shared way between the TAP functions of the plurality of components; and

selectively driving the TAP functions of the plurality of components with respective clocks.

2. The process of claim 1, comprising the operations of:

generating respective clocks for the TAP functions of the components of said plurality; and

associating, with said respective clocks, a pull-down function.

3. The process of claim 2, comprising the operations of providing a common line for application of said respective clocks to the TAP functions of the plurality of components.

4. The process of claim 2, comprising the operation of generating said respective clocks on board said single chip.

5. A system for management of a Test Access Port function in a plurality of components arranged on a single chip, each of the components provided with a respective TAP function adapted to be driven by a respective clock, comprising:

at least one line for use of at least one further signal in a shared way between the TAP functions of the plurality of components; and

at least one generator of a respective clock for selectively driving the TAP functions of the plurality of components.

6. The system of claim 5, comprising:

generators of respective clocks for the TAP functions of the plurality of components; and

at least one pull-down module associated with said respective clock generators.

7. The system of claim 6, comprising a common line for the application of said respective clocks to the TAP functions of the plurality of components.

8. The system of claim 6, wherein said clock generators are arranged on single chip.

9. A method of managing a Test Access Port (TAP) function in conjunction with a plurality of components on a single chip, comprising:

providing each component of the plurality of components with a respective TAP function;

providing each component of the plurality of components with a respective clock signal;

providing at least one shared line for use by at least one further signal among the TAP functions of the plurality of components; and

selectively driving the respective TAP functions of the plurality of components with the respective clock signals.

10. The method of claim 9, wherein providing each component with a respective clock signal comprises generating respective clock signals for the TAP functions of each component of the plurality of components.

11. The method of claim 10, wherein providing each component with a respective clock signal comprises associating with each respective clock signal a pull-down function.

12. The method of claim 11, wherein providing each component with a respective clock signal comprises providing a common line for use by each of the respective clock signals.

13. The method of claim 12, wherein each respective clock signal is generated onboard the single chip.

14. A system for managing testing of a plurality of components arranged on a single chip, the system comprising:

a Test Access Port function associated with each component of the plurality of components;

a plurality of clock generators, each clock generator associated with a respective TAP function for selectively driving the TAP function with a respective clock signal; and

at least one shared line coupled to each component of the plurality of components and configured to carry at least one further signal.

15. The system of claim 14, further comprising at least one pull-down module associated with each respective clock generator and configured to generate a pull-down function.

16. The system of claim 15, further comprising a common line coupled to each of the respective clock generators and to each of the respective components of the plurality of components for selectively carrying each of the respective clock signals.

17. The system of claim 16, wherein each of the plurality of clock generators are provided on the signal chip.